

REMARKS

Reconsideration and allowance of the subject application are respectfully requested.

Upon entry of this Amendment, claims 1-16 are pending in the application. In response to the Office Action (Paper No. 6), Applicant respectfully submits that the pending claims define patentable subject matter.

Claims 1-16 now rejected under 35 U.S.C. § 102(e) as being anticipated by Kaaresoja (U.S. Patent No. 6,556,573). Applicant respectfully traverses the claimed invention would not have been anticipated by or rendered obvious in view of the cited reference.

Kaaresoja discloses system and method for synchronizing variable bit rate traffic between a source and destination in an Asynchronous Transfer Mode (ATM) based GSM network. A variable bit rate ATM Adaptation Layer (AAL) protocol is designated to define ATM cell traffic flow from the source to the destination. A synchronous residual timestamp (SRTS) value indicative of the timing of a source clocking function is encoded and transmitted with an ATM cell using a variable bit rate AAL, such as AAL2 or AAL5. The ATM cells and associated SRTS values are received and decoded at the destination ATM interface, and the destination clock is synchronized with the source clock by modifying the destination clock according to the SRTS values.

As shown in Figure 1, an exemplary Base Station System (BSS) 100 includes Base Transceiver Stations (BTS) 102, 104 that communicate with associated Mobile Stations (MS) 106 and 108. A core network 114 interfaces with each BTS to route the information between the mobile stations and a Mobile Switching Center MSC 112. A transcoder (TC) or Inter Working

Function (IWF) 116 is provided between the core network 114 and MSC 112 to allow interoperation between a native protocol and an ATM-based device. The TC 116 can also be interfaced with other network environments, such as an Integrated Services Digital Network (ISDN) or the Public Switched Telephone Network (PSTN) 118. As shown in Figure 2, the BTS 200 may include pulse code modulation (PCM) oriented components 202, and an ATM interface 204 which interfaces to the core network 206. The IWF 208 includes an ATM interface 210, and a PCM interface 212 which interfaces to the MSC 214, the PSTN 216 or other PCM environment.

Although the Examiner generally cites various of portions of the Kaaresoja specification in support of the rejection without identifying any particular elements shown in the drawings of Kaaresoja which allegedly correspond to the claim elements, as best understood by the Application, the Examiner appears to be asserting the claimed first relay corresponds to the IWF (transcoder) 208, the claimed second relay corresponds to the BTS 200 and the claimed limited data rate transmission channel corresponds to the ATM core network 206.

However, Applicant respectfully submits that the ATM core network 206 is not a transmission channel having a limited data rate associated with the second protocol, as required by independent claims 1, 6, 12 and 13. Indeed, the protocol used for transmission in the ATM core network of Kaaresoja is the ATM protocol, which enables a very high data rate transmission, as is well known to those skilled in the art. On the contrary, in the present invention, the transmission channel is a limited data rate transmission channel, which means that

the protocol used for transmission on this channel (i.e. the “second protocol”) is different from a protocol like ATM or other protocol for transmission in packet mode.

In the example disclosed in the present application, the “second protocol” is the GSM protocol. More generally, the “second protocol” corresponds to a protocol for transmission in circuit mode (which, as opposed to packet mode, does not allow very high data rates, as known to the skilled person). In such a protocol, the present invention proposes to no longer transmit the data in a synchronous mode (such a synchronous mode being illustrated in the second row of Figure 3 of the present application) but to transmit the data in an asynchronous mode (such an asynchronous mode being illustrated in the third row of Figure 3 of the present application). Other than this change from synchronous mode to asynchronous mode, all other properties of this (second) protocol are kept the same. Accordingly, this does not mean that this (second) protocol is changed to, for example, the ATM protocol or another protocol in packet mode, and in particular, this does not mean that the transmission channel is therefore changed to a very high data rate transmission channel (i.e., this transmission channel remains a limited data rate transmission channel).

In addition, Applicant respectfully submits that Kaaresoja does not disclose “said data messages formatted in said second protocol include data messages having a length different from a length of a transmission window which would be used for transmission in the synchronous mode over said limited data rate transmission channel”, as further required by claim 12.¹

¹ The Examiner does not address this feature of claim 12 in the Office Action.

Further, Applicant respectfully submits that Kaaresoja does not disclose the subject matter of dependent claims 3 and 8 regarding receiving an instruction to retransmit a message. Although the Examiner cites column 8, lines 45-49 of Kaaresoja in support of the rejection of claims 3 and 8, the cited section of Kaaresoja does not mention receiving an instruction to retransmit a message.

Lastly, Applicant respectfully submits that Kaaresoja does not disclose the subject matter of claim 16. In particular, Kaaresoja nowhere teach or suggest “a decoder for receiving an instruction to retransmit a data message that has been previously stored in the buffer memory and transmitted in a synchronous mode to a receiver and based on the instruction, re-storing the data message to be retransmitted in the buffer memory or changing an order in which the data messages are read from the buffer memory.” Although the Examiner cites column 10, lines 44-49 and column 12, lines 10-60 for disclosing the claimed the decoder, Applicant respectfully submits that it is quite clear that the cited sections do not teach or suggest the claimed decoder for receiving an instruction to retransmit data messages, and storing the data messages that are to be retransmitted in the buffer memory or changing an order in which the data messages are read from the buffer memory.

Accordingly, Applicant respectfully submits that claims 1-16 should be allowable because the cited reference does not teach or suggest all of the features of the claims.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the

AMENDMENT UNDER 37 C.F.R. § 1.116
U.S. Patent Application No. 09/715,171

Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.


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